Remarks

Applicants thank Examiner Tsai for her careful examination of this application and her clear explanation of the claim rejections. Regarding the 102 rejections against claims 1-16, however, applicants respectfully submit that because the cited reference in the Office Action does not disclose all the elements in the rejected claims, the reference does not anticipate the claims, and the claims stand patentable over the cited reference:

Claim 1

Claim 1 describes a method of causing a test equipment to accurately place the edges of a signal used to test a device under test (DUT). The method includes at least the following steps that are not disclosed in the Miller patent:

a. determining an expected time of occurrence of each edge of the signal;

b. receiving data indicating a plurality of time points at which the edges of the signal have occurred in a plurality of cycles;

c. computing an error based on the plurality of time points and the expected time; and

d. adjusting the timing of the edges of the signal based on the error.

Regarding element (a), "determining an expected time of occurrence of each edge of the signal," the Office Action cites the following passages from the Miller patent:

> The test signal pattern of each channel is compared to a reference signal having the same edge pattern and the delay of each channel is adjusted to maximize cross-correlation between the test signal and the reference signal.[1]
>
> * * *
>
> HOST computer 30 also programs a reference signal generator 58 (suitably a spare tester channel) to produce a reference signal REF having a pattern similar to that of the TEST signal.[2]
>
> * * *

[1] US 6,606575, Abstract, ll. 4-6.
[2] Ibid. col. 8, ll. 3-6.

> While channel 26 and reference signal generator 52 are programmed to produce TEST and REF signals having similar pattern in response to the same CLOCK signal, the TEST and REF signals won't necessary arrive at compare circuit 60 in phase with one another.[3]

The cited passages disclose comparing TEST signals to REF signals and to maximize cross-correlation between the test signal and the reference signal; but there is no disclosure of determining an expected time of occurrence of either the TEST signal or the REF signal. The only requirement is that the reference signal REF have a pattern similar to that of the TEST signal. Applicants respectfully submit that there is no evidence in the cited passages that supports the argument that Miller discloses a specific step of "determining an expected time of occurrence of each edge of the signal."

Regarding element (b), "receiving data indicating a plurality of time points at which the edges of the signal have occurred in a plurality of cycles," the Office Action cites the following passage from the Miller patent:

> A test is organized into a succession of test cycles, and before the start of a test, host computer supplies a program to the control and timing circuit 46 within each channel 26 referencing the test event(s) to occur during each test cycle and indicating a time relative to the start of the test cycle that each event is to occur. During the test, each successive edge of the CLOCK signal marks the start of a test cycle. Test events include a change in state of a TEST signal output of driver 40 or an occurrence of an IC output signal (RESPONSE) state that is to be compared to the expect data. Thus in response to the program data from host computer 30, control and timing circuit 46 may respond to an edge of the CLOCK signal marking the start of a test cycle by enabling or tristating buffer 40 via a signal Z, by driving the buffer's input signal (DRIVE) high or low, and/or by supplying EXPECT data to comparator 43 and signaling acquisition system 44 via a COMPARE signal to sample the FAIL data. When control and timing circuit 46 is to change the state of the TEST signal during a test cycle, the program data for that test cycle indicates a nominal delay (a "programmable drive delay") following the start of the test cycle that the channel is to wait before changing the TEST signal state. Similarly, when control and timing circuit 46 is to signal acquisition system 44 to sample the FAIL signal during a test cycle, the program data for that test cycle indicates a nominal delay (a "programmable compare delay") following the

[3] Ibid. col. 8, ll. 20-24.

> start of the test cycle that the channel is to wait before signaling the acquisition system to sample the FAIL signal.[4]

This passage describes the prior art of how each channel in a tester tests a DUT based on a test program from the host computer. It describes how the RESPONSE data from the DUT are compared with EXPECT data in a comparator 43 following a finite "wait period" to determine the functionality of the DUT; there is no disclosure of the RESPONSE data indicating a plurality of time points at which the edges of the signal have occurred.

Applicants respectfully submit that there is no evidence in the cited passages that supports the argument that Miller discloses a specific step of "receiving data indicating a plurality of time points at which the edges of the signal have occurred in the plurality of cycles."

Regarding element (c), "computing an error based on said plurality of time points and the expected time." the Office Action cites the following passages from the Miller patent:

> As illustrated in FIG. 6, the calibration insert includes a compare circuit 60 for comparing the TEST and REF signals and producing an output MATCH signal. The MATCH output of compare circuit 60 indicates how well the amplitude of the TEST signal matches that of the REF signal. When both signals are high or both signals are low, the MATCH signal is high. When the TEST signal and the REF signals are of opposite states, the MATCH signal is low. Compare circuit 60 may be implemented by an XOR gate, but it is preferable to implement compare circuit 60 as an analog circuit, for example via an analog multiplier, so that the MATCH signal amplitude can fall anywhere within a continuous range of values depending on how well the TEST signal amplitude matches the REF signal amplitude.[5]
>
> * * *
>
> The phase deference between the two signals arises from differences in signal path lengths and in the inherent delays with which channel 26 and reference signal generator 58 respond to the CLOCK signal. The programmable drive calibration delay of control and timing circuit 46 also influences the phase difference between the TEST and REF signals calibration unit 52 processes the MATCH signal to provide cross-correlation data (CDATA) that is a measure of the phase difference

[4] Ibid. col. 5, ll. 14-39.
[5] Ibid. col. 8, ll. 6-19.

> between the TEST and REF signals. Host computer 30 calibrates the drive delay of tester channel 26 by iteratively adjusting the calibration data input to control and timing circuit 46 until the CDATA indicates that the TEST signal is in phase with the REF signal.[6]

These passages disclose the procedure of matching the TEST and REF signals. In the paragraph that follows the cited paragraphs, the matching is accomplished by integrating the MATCH signal;[7] not based on any plurality of time point, and they do not disclose any expect time. Therefore, there can not be any computing of an error based on the two.

Applicants respectfully submit that there is no evidence in the cited passages that supports the argument that Miller discloses a specific step of "computing an error based on a plurality of time points and the expected time."

Regarding element (d), "adjusting a timing of the edges of the signal based on the error," the Office Action cites the following passages from the Miller patent:

> The test signal pattern of each channel is compared to a reference signal having the same edge pattern and the delay of each channel is adjusted to maximize cross-correlation between the test signal and the reference signal.[8]
>
> * * *
>
> Host computer 30 calibrates the drive delay of tester channel 26 by iteratively adjusting the calibration data input to control and timing circuit 46 until the CDATA indicates that the TEST signal is in phase with the REF signal.[9]

The Miller patent discloses calibration the channel to match the TEST and REF signals; but it does not disclose adjusting timing of a signal edge based on the error signal described in applicants' application because of the reason relating to element (c). Applicants respectfully submit that there is no evidence in the cited passages that supports the argument that Miller discloses a specific step of "adjusting a timing of the edges of a signal based on the error."

---

[6] Ibid. col. 8, ll. 24-33.
[7] Ibid. col. 8, ll. 57-59.
[8] Ibid. Abstract, ll. 4-6.
[9] Ibid. col. 8, ll. 33-37.

In summary, applicants respectfully submit that because the Miller patent does not disclose at least the elements (a), (b), (c), and (d) in claim 1 of the instant applicant, the Miller patent can not anticipate claim 1 and claim 1 stands patentable over the Miller patent.

Claims 2-8

Claims 2-8 properly depend from claim 1 with additional elements of limitation. In particular, claim 2 further limits the relationship of the expected time and the time points of the signals and a tester cycle time of the test equipment; claim 3 further limits the smallest number of the time points; claim 4 further includes a command to configure the DUT interface board; claim 5 further includes a step of setting an acceptable limit for the error; claim 6 further limits the computing step; claim 7 further includes the instruction step of setting the signal edges; and claim 8 further includes the instruction step of sending a threshold voltage level to compare to the signals. Applicants respectfully submit that claims 10-16 stand patentable over the Miller patent at least by virtue of their dependence.

Claim 9

Claim 9 describes a readable medium that carries sequences of instructions for causing a digital processing system to control a test equipment to accurately place the edges of a signal used to test a device under test (DUT). The sequences include at least the following executable steps that are not disclosed in the Miller patent:

a. determining an expected time of occurrence of each edge of a signal;

b. receiving data indicating a plurality of time points at which the edges of the signal have occurred in a plurality of cycles;

c. computing an error based on the plurality of time points and the expected time; and

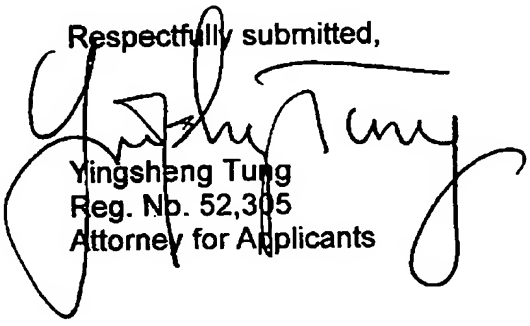
d. adjusting a timing of the edges of the signal based on the error.

The passages cited in the Office Action as evidence that the Miller patent anticipates claim 9 are the same as those against claim 1. For the same reason submitted above relating to claim 1, the cited reference does not disclose steps (a), (b), (c), and (d) in claim 9. Therefore, applicants respectfully submit that the Miller patent does not anticipate claim 9 and claim 9 stands patentable over the Miller patent.

Claims 10-16

Claims 10-16 properly depend from claim 9 with additional elements of limitation. In particular, claim 10 further limits the relationship of the expected time and the time points of the signals and a tester cycle time of the test equipment; claim 11 further limits the smallest number of the time points; claim 12 further includes a command to configure the DUT interface board; claim 13 further includes a step of setting an acceptable limit for the error; claim 14 further limits the computing step; claim 15 further includes the step of setting the signal edges; and claim 16 further includes the step of sending a threshold voltage level to compare to the signals. Applicants respectfully submit that claims 10-16 stand patentable over the Miller patent at least by virtue of their dependence.

Respectfully submitted,



Yingsheng Tung
Reg. No. 52,305
Attorney for Applicants

Texas Instruments Incorporated
P. O. Box 655474 MS 3999
Dallas, TX 75264
(972) 917-5355